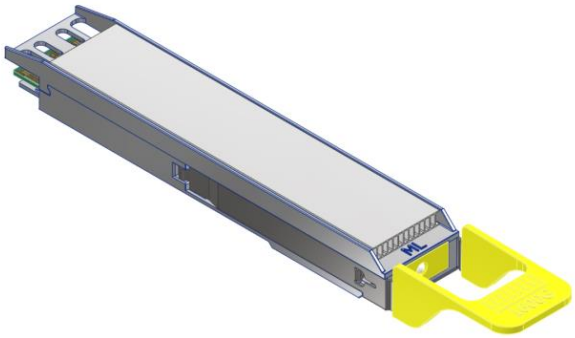
multiLane

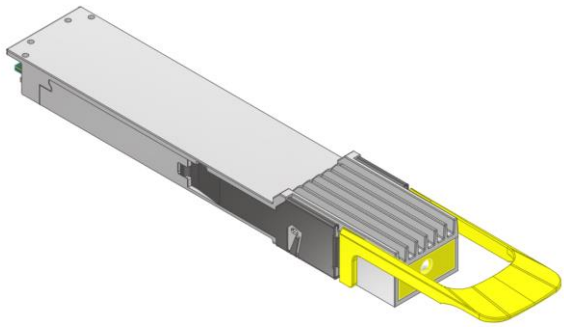
ML4064-LB2-224

Technical Reference

OSFP Electrical Passive Loopback Module

CMIS 5.2 Compliant





Innovation for the next generation

Table of Contents

ML4064-LB2-224 OSFP 8x224G Passive Loopback Module - Key Features

- ✓ Loops back TX & RX with good performance SI Traces
- ✓ Built with advanced PCB Material
- ✓ MSA Compliant Shell with latching mechanism
- ✓ Can dissipate up to 45W
- ✓ Supports I2C and I3C interfaces
- ✓ Implements CMIS Memory Map with programmable new pages
- ✓ Ability to control/ monitor all low-speed signals
- ✓ Four temperature sensors (2 through- hole and 2 SMT)
- ✓ Two Inrush and Current sensors are used to cover the power needed
- ✓ Two Voltage sensors on the 3.3V (one for each inrush sensor)
- ✓ True Insertion Counter
- ✓ Available in Type2 IHS and RHS shells
- ✓ Hot Pluggable
- ✓ Cut-off temperature preventing module overheating

LED Indicator

Green (Solid) – Signifies that the module is operating in high power mode.
Red (Solid) – Signifies the module is operating in low power mode.
Green (Blinking) – Module in high power mode and Voltage or Temperature Alarm is triggered.
Red (Blinking) – Module in Low power mode and Voltage or Temperature Alarm is triggered.

Recommended Operating Conditions

Parameter	Symbol	Notes/Conditions	Min	Type	Max	Units
Operating Temperature	T_A		0		85	°C
Supply Voltage	VCC	Main Supply Voltage	2.97	3.3	3.63	V
Power Class		Programmable to Emulate all power classes	0		45	W
Data Rate	Rb	Guaranteed to work at 224Gbps per lane			1600	Gbps

1. General Description

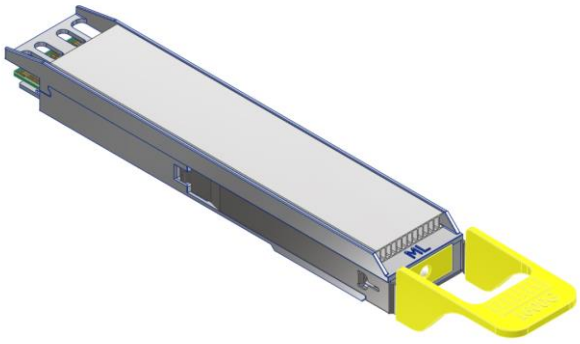
The **ML4064-LB2-224** is an OSFP passive electrical loopback module which is a hot pluggable form factor designed for high-speed testing application for OSFP host ports. The **ML4064-LB2-224** is designed for **1.6 Terabits** Ethernet applications and provides **8x224G RX** and **TX lanes**, **I2C** module management interface and all the OSFP hardware signals.
The **ML4064-LB2-224** loops back 8-lane **224** Gbps transmit data from the Host back to 8-lane **224Gbps** receive data port to the Host.
The **ML4064-LB2-224** provides programmable power dissipation up to 45W allowing the module to emulate all the OSFP power classes. It also provides an insertion counter, a LED blinking rate, an upper temperature cut-off and a temperature sensor.

2. Ordering Information

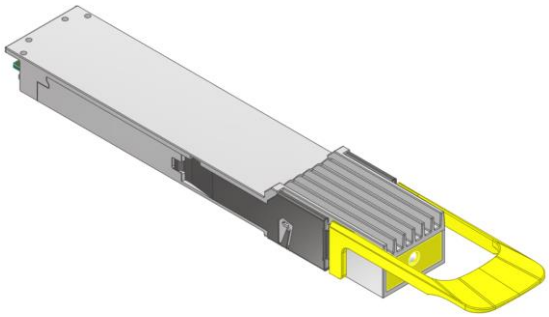
2.1 Ordering options

The ordering options of the ML4064-LB2-224 are detailed in the table below:

Option	Part Number	Description
#1 – IHS	ML4064-LB2I-224	OSFP IHS shell option
#2 – RHS	ML4064-LB2R-224	OSFP RHS shell option



IHS



RHS

3. Functional Description

3.1 I2C Signals, Addressing and Frame Structure

3.1.1 I2C Frame

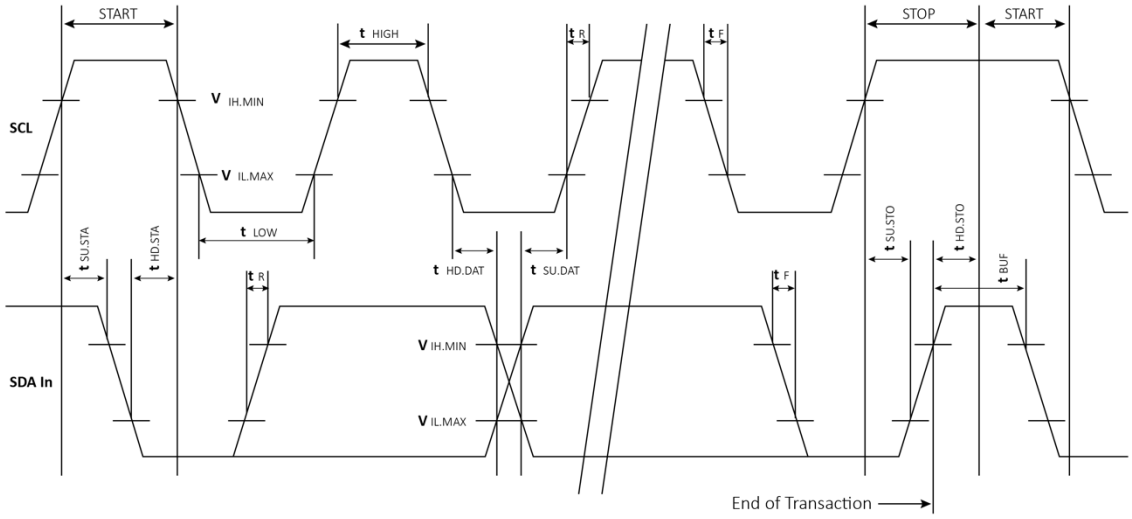


Figure 1: OSFP Timing Diagram

3.1.2 Management Timing Parameters

The timing parameters for the 2-Wire interface to the OSFP module are shown in the table below:

Parameter	Symbol	Min	Max	Unit
Clock Frequency	f_{SCL}		400	kHz
Clock Pulse Width Low	t_{LOW}	1.2		us
Clock Pulse Width High	t_{High}	1.1		us
Time bus free before new transmission can start	t_{BUF}	20.8		us
Input Rise Time (400kHz)	$T_{R,400}$		300	ns
Input Fall Time (400kHz)	$T_{F,400}$		300	ns
Serial Interface Clock HoldOff (Clock Stretching)	T_Clock_hold		500	us

Maximum time the OSFP Module may hold the SCL line low before continuing with a read or write operation is 500us.

3.1.3 Device Addressing and Operation

Serial Clock (SCL): The host supplied SCL input to OSFP transceivers is used to positive-edge clock data into each OSFP device and negative-edge clock data out of each device.

Serial Data (SDA): The SDA pin is bi-directional for serial data transfer. This pin is open-drain or open-collector driven.

Master/Slave: OSFP transceivers operate only as slave devices. The host must provide a bus master for SCL and initiate all read/write communication.

Device Address: Each OSFP is hard wired at the device address A0h.

Clock and Data Transitions: The SDA pin is normally pulled high with an external device. Data on the SDA pin may change only during SCL low time periods. Data changes during SCL high periods indicating a START or STOP condition. All addresses and data words are serially transmitted to and from the OSFP in 8-bit words. Every byte on the SDA line must be 8-bits long. Data is transferred with the most significant bit (MSB) first.

START Condition: A high-to-low transition of SDA with SCL high is a START condition, which must precede any other command.

STOP Condition: A low-to-high transition of SDA with SCL high is a STOP condition.

Acknowledge: After sending each 8-bit word, the transmitter releases the SDA line for one-bit time, during which the receiver is allowed to pull SDA low (zero) to acknowledge (ACK) that it has received each word. Device address bytes and write data bytes initiated by the host are acknowledged by OSFP transceivers. Read data bytes transmitted by OSFP transceivers should be acknowledged by the host for all but the final byte read, for which the host should respond with a STOP instead of an ACK.

Memory (Management Interface) Reset: After an interruption in protocol, power loss or system reset the OSFP management interface can be reset. Memory reset is intended only to reset the OSFP transceiver management interface (to correct a hung bus). No other transceiver functionality is implied.

1. Clock up to 9 cycles
2. Look for SDA high in each cycle while SCL is high
3. Create a Start condition as SDA is high

Device Addressing: OSFP devices require an 8-bit device address word following a start condition to enable a read or write operation. The device address word consists of a mandatory sequence for the first seven most significant bits in Figure 1. This is common to all OSFP devices.

1	0	1	0	0	0	0	R/W
MSB							LSB

Figure 2: OSFP Device Address

The eighth bit of the device address is the read/write operating select bit. A read operation is initiated if this bit is set high and a write operation is initiated if this bit is set low. Upon compare of the device address the OSFP transceiver output a zero (ACK) on the SDA line to acknowledge the address.

3.2 I2C Read/Write Functionality

3.2.1 OSFP Memory Address Counter (Read and Write Operations)

OSFP devices maintain an internal data word address counter containing the last address accessed during the latest read or write operation, incremented by one. The address counter is incremented whenever a data word is received or sent by the module. This address stays valid between operations as long as OSFP power is maintained. The address "roll over" during read and writes operations is from the last byte of the 128-byte memory page to the first byte of the same page.

3.2.2 Read Operations

A. Current Address Read

A current address read operation requires only the device address read word (10100001) be sent, see Figure 2 below.

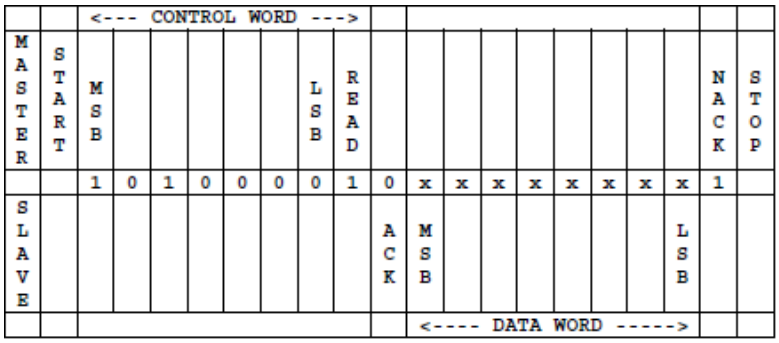


Figure 3: OSFP Current Address Read Operation

Once acknowledged by the OSFP, the current address data word is serially clocked out. The host does not respond with an acknowledgement, but does generate a STOP condition once the data word is read.

B. Random Read

A random read operation requires a "dummy" write operation to load in the target byte address as shown in Figure 3 below. This is accomplished by the following sequence.

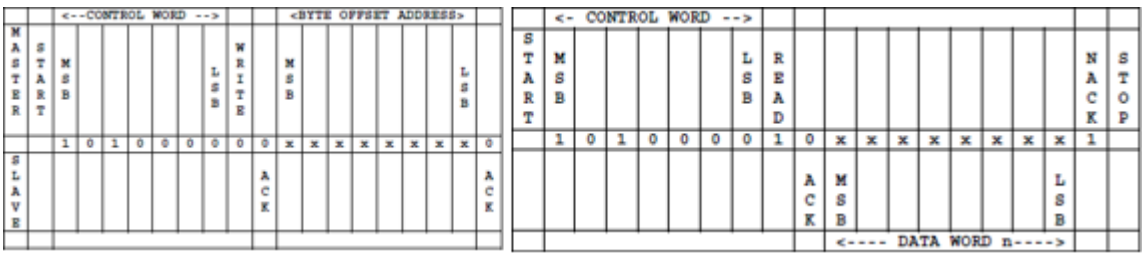


Figure 4: OSFP Random Read

The target 8-bit data word address is sent following the device address write word (10100000) and acknowledged by the OSFP. The host then generates another START condition (aborting the dummy write without incrementing the counter) and a current

address read by sending a device read address (10100001). The OSFP acknowledges the device address and serially clocks out the requested data word. The host does not respond with an acknowledgement, but does generate a STOP condition once the data word is read.

C. Sequential Read

Sequential reads are initiated by a current address read (Figure 4). To specify a sequential read, the host responds with an acknowledgement (instead of a STOP) after each data word. As long as the OSFP receives an acknowledgement, it will serially clock out sequential data words.
The sequence is terminated when the host responds with a NACK and a STOP instead of an acknowledgement.

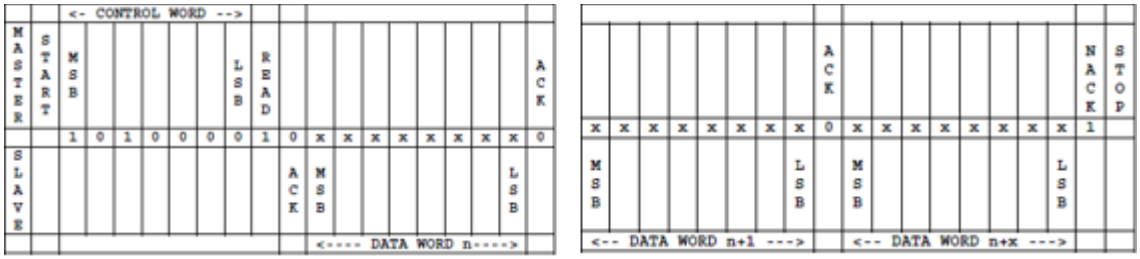
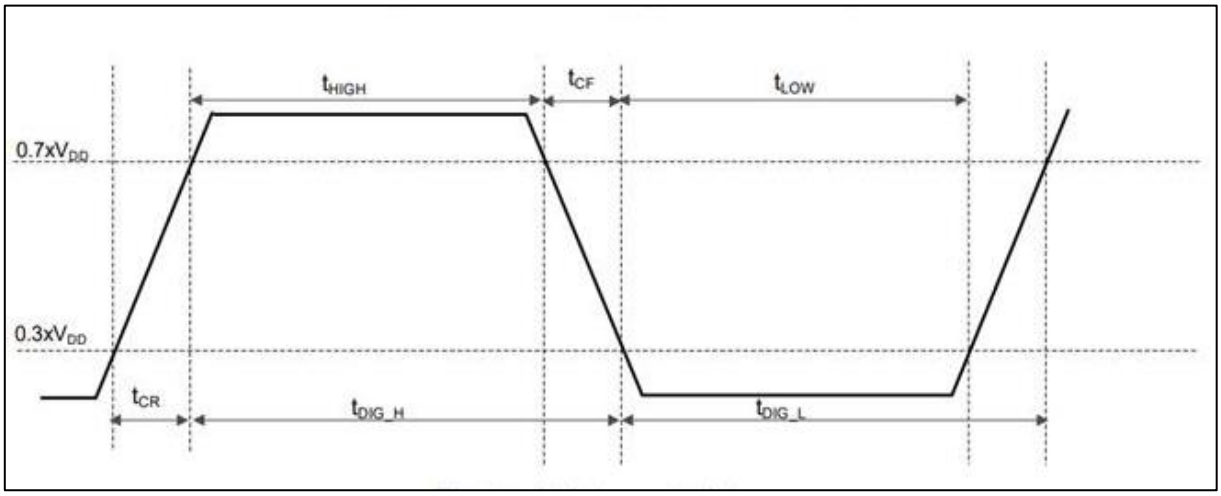


Figure 5: Sequential Address Read Starting at OSFP Current Address

3.3 I3C

3.3.1 I3C Timing



3.3.2 Management Timing Parameters

I3C Push–Pull timing Parameters at 12.5 MHz

Parameter	Symbol	Min	Max	Units
SCL Clock Frequency	f_{SCL}	0.01	12.9	MHz
SCL Clock Low Period	t_{LOW}	24	-	ns
	t_{DIG_L}	32	-	ns
SCL Clock High Period (for Pure Bus)	t_{HIGH}	24	-	ns
	t_{DIG_H}	32	-	ns
Clock in to Data Out for Target	t_{sco}	-	12	ns
SCL Clock Rise Time	t_{CR}	8	12	ns
SCL Clock Fall Time	t_{CF}	6	12	ns
SDA Signal Data Hold in Push-Pull Mode - Target	t_{HD_PP}	0	-	ns
SDA Signal Data Setup in Push-Pull Mode	t_{SU_PP}	3	-	ns

I3C Open–Drain timing Parameters

Parameter	Symbol	I3C Open Drain Mode	Min	Max	Units
Low Period of SCL Clock	t_{LOW_OD}		200	-	ns
	$t_{DIG\_OD\_L}$	$t_{LOW\_ODmin} + t_{DA\_ODmin}$	-	-	ns
High Period of SCL Clock (Pure Bus)	t_{HIGH}		24	-	ns
	t_{DIG_H}	t_{DIG_Hmin} from Push-Pull	32	-	ns
SDA Data Setup Time During Open Drain Mode	t_{SU_OD}		3	-	ns
Clock After START (S) Condition	t_{CAS}	For ENTAS0: 1 µs, ENTAS1: 100 µs, ENTAS2: 2 ms, ENTAS3: 50 ms	38.4 ns	-	s

3.3.3 Device Addressing and Operation

The Improved Inter-Integrated Circuit (I3C) is a next-generation serial communication interface developed by the MIPI Alliance. It addresses the limitations of legacy interfaces I2C while introducing advanced features for high-speed, efficient, and scalable communication.
Key Features of I3C:

- High-Speed Communication: I3C supports clock speeds up to 12.5 MHz in Standard Data Rate (SDR) mode.
- Dynamic Addressing: I3C dynamically assigns addresses, reducing the risk of collisions and improving bus management.
- In-Band Interrupts (IBI): module can signal interrupts directly on the bus without requiring additional GPIO lines.

- Hot-Join Capability: Devices can join or leave the bus dynamically, enabling hot-swappable components.
- Backward Compatibility: I3C supports mixed bus operation, allowing legacy I2C devices to coexist with I3C devices.
- Push-Pull and Open-Drain Modes: I3C automatically switches between these modes for efficient communication.

3.3.4 I3C Target Supported Features

I3C target is implemented on Multilane modules, below is the table of implementations:

Feature	Implementation	Notes
Common Command Codes (CCCs)	Implemented	CCCs such as RSTDAA, ENTDAA, ENEC, DISEC, SETMWL, SETMRL, GETMWL, GETMRL, GETBCR, GETSTATUS are all implemented.
I3C SDR mode Private read and write	Implemented	It is Tested on several Push – Pull speeds (3.75 MHz, 5 MHz, 6.25 MHz, 7.5 MHz, 10 MHz, 12.5 MHz), and on several Open Drain speeds (100 KHz, 250 KHz, 500 KHz, 1.25 MHz, 2.5 MHz, 3.125 MHz).
Hot-Join	Implemented	It is initialized as disabled and can be enabled by host and used after MCU reset.
In-band Interrupt	Not fully implemented	It has been tested with dummy data only. Need customer requirements.
Continuous read and write frame	Implemented	Tested on 2048 bytes of payload.
CDB	Implemented	FW upload through EPL Write CMD.

3.4 Password Protected Space

The memory space protected by password is RO, and can be written after successful password entry.

Password should be entered in Registers 122 to 125 (4 bytes) in low memory.
The default password is (in hex): 00 00 10 11.

The password can be changed in Registers 118 to 121.

Address	Bits	Name	Description	Type
118 – 121	7-0	Password Change Entry Area		WO
122 – 125	7-0	Password Entry Area		WO

The registers protected by Password are listed in the following table:

Page	Address	Description
Low Memory	0-2	ID and Status Area
	85-90	Application advertisement

	118-121	Password Change
Page 00	128-200	Identifier
	202-212	Vendor information Date code Module power characteristics
Page 01	176	Advertisement
Page 02	128-143	Alarm thresholds

3.5 OSFP Memory Map

3.5.1 ML4064-LB2-224 Memory Map

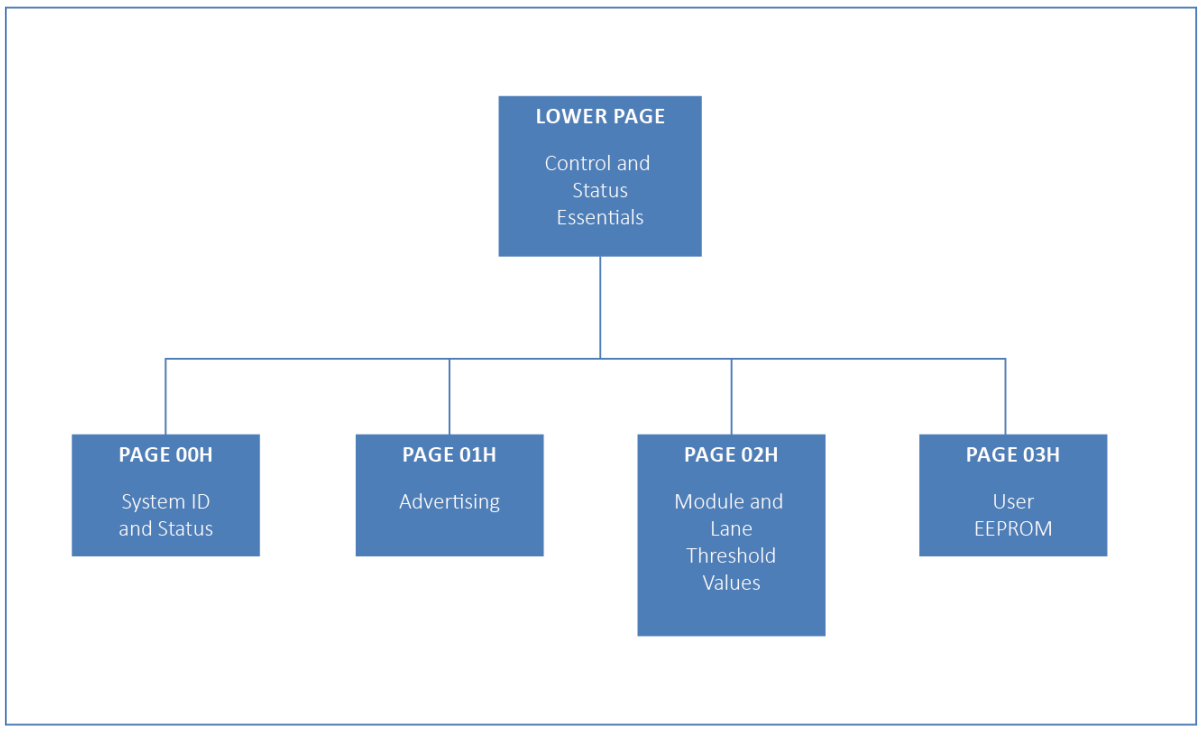


Figure 6: Implemented Memory

3.5.2 Memory Accessibility

The Memory Map registers types are shown in the table below:

Page Address	Address Range	Type
Lower Page	0-25	RO
	26	RW (VR)
	27-126	RO
	127	RW (VR)
Page 00h	128-165	RO
	166-181	RW (NVR)
	182-255	RO
Page 01h	128-255	RO
Page 02h	128-255	RO
Page 03 Lower Page	128-224	RW (NVR)
	225-246	RO
	247-253	RW (NVR)

	254	RW(VR)
	255	RW(VR)

3.5.3 Memory Content

The table below shows the memory content.

Page	Address	Hex	ASCII	CMIS Description	Type
Low Memory	0	0x19		SFF8024Identifier	RO
	1	0x52		CMIS Revision	RO
	2	0x04		MemoryModel, SteppedConfigOnly and i2c speed	RO
	3	0x07		Global Status Information	RO
	4-7	0		NA	RO
	8	0		State machine change flag indicator	RO
	9	0		Vcc, Temp Alarm and warning	RO
	10	0		NA	RO
	11	0		custom monitor alarm and threshold	RO
	12	0		reserved	RO
	13	0		custom	RO
	14	0		TempMonValue MSB	RO
	15	0		TempMonValue LSB	RO
	16	0		VccMonValue MSB	RO
	17	0		VccMonValue LSB	RO
	18	0		Aux1MonValue MSB	RO
	19	0		Aux1MonValue LSB	RO
	20-23	0		NA	RO
	24	0		CustomMonValue MSB	RO
	25	0		CustomMonValue LSB	RO
	26	0x40		Module Global Controls	RW VR
	27	0		reserved	RO
	28	0		reserved	RO
	29	0		custom	RO
	30	0		custom	RO
	31-34	0		NA	RO
	35	0		reserved	RO
	36	0		custom	RO
	37	0		NA	RO
	38	0		NA	RO
	39	1		ModuleActiveFirmwareMajorRevision	RO
	40	0		ModuleActiveFirmwareMinorRevision	RO
	41	0		NA	RO
	42-63	0		reserved	RO
	64-84	0		custom	RO
	85	0x03		MediaType	RO
	86	0x80		HostInterfaceID	RO
	87	0xBF		MediaInterfaceID	RO
	88	0x88		HostLaneCount and MediaLaneCount	RO

	89	0x01		HostLaneAssignmentOptions	RO
	90	0xFF		end of application	RO
	91-126	0		NA	RO
	127	0		PageSelect	RW VR
PAGE 00	128	0x19		SFF8024IdentifierCopy	RO
	129	0x4D	M	VendorName	RO
	130	0x55	U		RO
	131	0x4c	L		RO
	132	0x54	T		RO
	133	0x49	I		RO
	134	0x4c	L		RO
	135	0x41	A		RO
	136	0x4e	N		RO
	137	0x45	E		RO
	138	0x20			RO
	139	0x20			RO
	140	0x20			RO
	141	0x20			RO
	142	0x20			RO
	143	0x20			RO
	144	0x20			RO
	145	0		Vendor OUI	RO
	146	0			RO
	147	0			RO
	148	0x34	4	VendorPN	RO
	149	0x30	0		RO
	150	0x36	6		RO
	151	0x34	4		RO
	152	0x4c	L		RO
	153	0x42	B		RO
	154	0x32	2		RO
	155	0x49	I		RO
	156	0x2d	-		RO
	157	0x32	2		RO
	158	0x32	2		RO
	159	0x34	4		RO
	160	0x20			RO
	161	0x20			RO
	162	0x20			RO
	163	0x20			RO
	164	0x31	1	VendorRev	RO
	165	0x30	0		RO
	166-181	0x20		VendorSN	RW NVR
	182	0x32		DateCode	RO
	183	0x35			RO
	184	0x30			RO

	185	0x33			RO
	186	0x30			RO
	187	0x34			RO
	188	0x30			RO
	189	0x31			RO
	190-199	0		CLEICode	RO
	200	0xE0		ModulePowerClass	RO
	201	0xB4		MaxPower	RO
	202	0x00		Cable Assembly Link Length	RO
	203	0x00		ConnectorType	RO
	204	0x00		AttenuationAt5GHz	RO
	205	0x00		AttenuationAt7GHz	RO
	206	0x00		AttenuationAt12p9GHz	RO
	207	0x00		AttenuationAt25p8GHz	RO
	208	0x00		reserved	RO
	209	0x00		reserved	RO
	210	0x00		Media Lane Information	RO
	211	0x00		Cable Assembly Information	RO
	212	0x08		MediaInterfaceTechnology	RO
	213-220	0x00		reserved	RO
	221	0x00		custom	RO
	222	0x91		PageChecksum	RO
	223-255	0x00		custom information	RO
PAGE 01	128	0		ModuleInactiveFirmwareMajorRevision	RO
	129	0		ModuleInactiveFirmwareMinorRevision	RO
	130	0x01		ModuleHardwareMajorRevision	RO
	131	0x01		ModuleHardwareMinorRevision	RO
	132-141	0		NA	RO
	142	0x04		Supported Pages Advertising	RO
	143	0x00		ModSelWaitTime	RO
	144	0x00		MaxDurationDPDeinit and MaxDurationDPInit	RO
	145	0x00		Module Characteristics Advertising	RO
	146	0x55		ModuleTempMax	RO
	147	0xd8		ModuleTempMin	RO
	148	0		NA	RO
	149	0		NA	RO
	150	0x87		OperatingVoltageMin	RO
	151	0		NA	RO
	152	0		NA	RO
	153	0		RxOutputLevel Supported and TxInputEqMax	RO
	154	0		RxOutputEqPostCursorMax and RxOutputEqPreCursorMax	RO
	155	0		Media side Supported Controls Advertisement	RO
	156	0		Host side Supported Controls Advertisement	RO
	157	0		NA	RO

	158	0		CDRLOLFlagRxSupported LOSFlagRxSupported	RO
	159	0x27		Supported Monitors Advertisement	RO
	160	0		NA	RO
	161	0		TxInput Eq Supports	RO
	162	0		pre post amplitude supported	RO
	163	0x57		CDB Advertisement	RO
	164	0xFF		CdbReadWriteLengthExtension	RO
	165	0x04		CdbCommandTriggerMethod	RO
	166	0x80		CdbMaxBusySpecMethod	RO
	167	0		MaxDurationModulePwrDn/Up	RO
	168	0		MaxDurationDPTxTurnOff/On	RO
	169-175	0		reserved	RO
	176	0x01		complementary of app sel 1	RO
	177-190	0		NA	RO
	191-222	0		custom	RO
	223-250	0		NA	RO
	251-254	0		reserved	RO
	255	0xCE		check sum of page01	RO
PAGE 02	128	0x50		TempMonHighAlarmThreshold	RO
	129	0			RO
	130	0		TempMonLowAlarmThreshold	RO
	131	0			RO
	132	0x4B		TempMonHighWarningThreshold	RO
	133	0			RO
	134	0x05		TempMonLowWarningThreshold	RO
	135	0			RO
	136	0x8D		VccMonHighAlarmThreshold	RO
	137	0xCC			RO
	138	0x74		VccMonLowAlarmThreshold	RO
	139	0x04			RO
	140	0x8B		VccMonHighWarningThreshold	RO
	141	0xD8			RO
	142	0x75		VccMonLowWarningThreshold	RO
	143	0xF8			RO
	144-199	0		NA	RO
	200-229	0		reserved	RO
	230-254	0		custom	RO
	255	0X41		Page 2 checksum	RO
PAGE 03	128-224	0		User EEPROM	RW NVR
	225 (PAGE 03)	0		INT/RSTn analog MSB	RO
	226 (PAGE 03)	0		INT/RSTn analog LSB	RO
	227 (PAGE 03)	0		LPWn/PRSn analog MSB	RO
	228 (PAGE 03)	0		LPWn/PRSn analog LSB	RO
	229 (PAGE 03)	0		TempSens 1 MSB	RO
	230 (PAGE 03)	0		TempSens 1 LSB	RO

	231 (PAGE 03)	0		TempSens 2 MSB	RO
	232 (PAGE 03)	0		TempSens 2 LSB	RO
	233 (PAGE 03)	0		TempSens 3 MSB	RO
	234 (PAGE 03)	0		TempSens 3 LSB	RO
	235 (PAGE 03)	0		TempSens 4 MSB	RO
	236 (PAGE 03)	0		TempSens 4 LSB	RO
	237 (PAGE 03)	0		VoltSens 1 MSB	RO
	238 (PAGE 03)	0		VoltSens 1 LSB	RO
	239 (PAGE 03)	0		VoltSens 2 MSB	RO
	240 (PAGE 03)	0		VoltSens 2 LSB	RO
	241 (PAGE 03)	0		CurrentSens 1 MSB	RO
	242 (PAGE 03)	0		CurrentSens 1 LSB	RO
	243 (PAGE 03)	0		CurrentSens 2 MSB	RO
	244 (PAGE 03)	0		CurrentSens 2 LSB	RO
	245 (PAGE 03)	0		true insertion counter MSB	RO
	246 (PAGE 03)	0		true insertion counter LSB	RO
	247 (PAGE 03)	0		Power Register 1	RW NVR
	248 (PAGE 03)	0		Power Register 2	RW NVR
	249 (PAGE 03)	0		Power Register 3	RW NVR
	250 (PAGE 03)	0		Power Register 4	RW NVR
	251 (PAGE 03)	0		Power Register 5	RW NVR
	252 (PAGE 03)	0		Power Register 6	RW NVR
	253 (PAGE 03)	0x55		temp cutoff	RW NVR
	254 (PAGE 03)			Init Mode state	RW VR
	255 (PAGE 03)			Digital control of INTL	RW VR

3.6 Low Speed Electrical Hardware Pins

In addition to the 2-wire serial interface the module has the following low speed pins for control and status.

3.6.1 INT/RSTn

INT/RSTn is a dual function signal that allows the module to raise an interrupt to the host and also allows the host to reset the module.
Reset is an active low signal on the host which is translated to an active low signal on the module.
Interrupt is an active high signal on the module which gets translated to an active low signal on the host.

3.6.2 LPWn/PRSn

LPWn/PRSn is a dual function signal that allows the host to signal Low Power mode and the module to indicate Module Present.
Low Power mode is an active low signal on the host which gets converted to an active low signal on the module.
Module Present is controlled by a pull-down resistor on the module which gets converted to an active low logic signal on the host.

3.7 ML4064-LB2-224 Specific Functions

3.7.1 Module State

The Module State describes module-wide behaviors and properties. The **ML4064-LB2-224** implements two module states: ModuleLowPwr and ModuleReady.
The ModuleLowPwr state is a host control state, where the management interface is fully initialized and operational and the Module is in Low Power mode, where the Power Spots are deactivated. During this state, the host may configure the module using the management interface and memory map. The module state encoding for ModuleLowPwr is 001.
The ModuleReady state is a host control state that indicates that the module is in High Power mode, and the PWM is activated. The module state encoding for ModuleReady is 011.

Address	Bit	Name	Description	Type
3 (lower Page)	3~1	Module State	Current state of Module: 001b= ModuleLowPwr 011b= ModuleReady	RO

3.7.2 Module State Transition

The state transition between Low Power and High Power is related to three parameters:
1. ForceLowPwr bit– software control (forces module into low power mode), register 26 bit 4
2. LowPwr bit – software control, register 26 bit 6
3. LPMode – Hardware signal

According to these parameters, the state of the module is defined. Conditions for Low Power and High Power state, are summarized in the table below.

ForceLowPwr (Reg 26 bit 4)	LowPwr (register 26 bit 6)	LPMode	State
1	X	X	Low Power
0	1	1	Low Power
0	1	0	High Power
0	0	1	High Power
0	0	0	High Power

3.7.3 Module Global Controls

Module global controls are control aspects that are applicable to the entire module on all channels in the module.

Address	Bit	Name	Description	Type
26(lower Page)	6	LowPwr	Parameter used to control the module power mode Default value =1	RW
	4	ForceLowPwr	0b = high power mode(default) 1b =Forces module into low power mode	
	3	Software Reset	Self-clearing bit that causes the module to be reset. The effect is the same as asserting the reset pin for the appropriate hold time, followed by its de-assertion. This bit will be cleared to zero on a reset	

			so a value of 0 will always be returned. 0b = not in reset 1b = Software reset	
3(lower page)	0	Software Interrupt	Digital state of Interrupt: 0b = Interrupt source is present 1b = No interrupt source present	RO

3.7.4 Voltage Sense

A voltage sense circuit is available allowing the measure of internal module supplied voltage Vcc. Supply voltage is represented as a 16-bit unsigned integer with the voltage defined as the full 16-bit value (0 – 65535) in increments of 100 µV, yielding a total measurement range of 0 to +6.55 Volts.

Address	Bit	Name	Description	Type
16	All	Supply voltage MSB	Internally measured supply voltage	RO
17	All	Supply voltage LSB	Internally measured supply voltage	

The Voltage alarms and warnings interrupt flags exists in lower page.

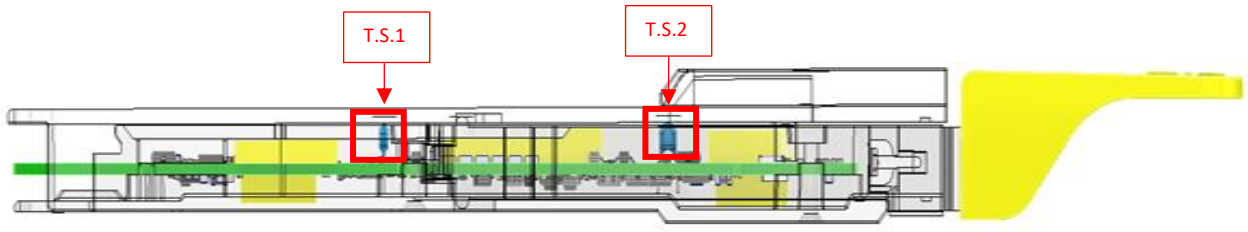
Address	Bit	Name	Description	Type
9 (lower Page)	7	L-Vcc3.3v Low Warning	Latched low 3.3 volts supply voltage warning flag	RO
	6	L-Vcc3.3v High Warning	Latched low 3.3 volts supply voltage warning flag	
	5	L-Vcc3.3v Low Alarm	Latched low 3.3 volts supply voltage alarm flag	
	4	L-Vcc3.3v High Alarm	Latched low 3.3 volts supply voltage alarm flag	

3.7.5 Temperature sense

The **ML4064-LB2-224** has 2 temperature sensors on the PCBA to continuously monitor the module temperature. Internally measured Module temperatures are represented as a 16-bit signed two's complement value in increments of 1/256 degrees Celsius, yielding a total range of –127°C to +128°C that is considered valid between –40° and +125° C.

Address	Bit	Name	Description	Type
14 Lower Page	All	Temperature Sense 1 MSB	Case Temperature	RO
15 Lower Page	All	Temperature Sense 1 LSB		
18 Lower Page	All	Temperature Sense 2 MSB	Internally measured temperature	
19 Lower Page	All	Temperature Sense 2 LSB		

The distribution of internal temperature sensors is shown in the figure below.



The temperature alarms and warnings interrupt flags exist in lower page:

Address	Bit	Name	Description	Type
9 (lower Page)	3	L-Temp Low Warning	Latched low temperature warning flag	RO
	2	L-Temp High Warning	Latched high temperature warning flag	
	1	L-Temp Low Alarm	Latched low temperature alarm flag	
	0	L-Temp High Alarm	Latched high temperature alarm flag	

Note that any interrupt flag when asserted will generate the interrupt. Its state is read from register 3 bit 0.

3.7.6 Cut-Off Temperature

To avoid overheating the module, a Cut-Off Temperature is pre-defined.
The module is continuously monitoring the temperature and checking its value against the Cut-Off temperature. Once the module temperature reaches the cut-off temperature, the PWM will automatically turn off in order to prevent overheating. Once the temperature is 5 degrees below cut-off value, the PWM goes back to its previous value.
The maximum Cut-Off temperature for the **ML4064-LB2-224** is 100° C and it can be programmed to any value from register 253 of memory page 03. Its default value is 100° C.

Address	Bit	Name	Description	Type
253	7:0	Cut-Off temperature	Module Cut-Off Temperature, LSB = 1 degC	RW (NVR)

3.7.7 Current Sense

A current sense circuit is available in the ML4064-LB2-224 that allows monitoring the current consumption of the heaters that are distributed over six power spots. The current sense is able to measure up to 12 Amps. Current is stored on page 03 registers 241-242 and 243-244, and combined current sense is stored in low memory registers 24 and 25

Address	Bit	Name	Description	Type
24	All	CustomMonValue MSB	Current consumption in mA	RO
25	All	CustomMonValue LSB		
241 (page 03)	All	Current Consumption 1 MSB		
242 (page 03)	All	Current Consumption 1 LSB		
243 (page 03)	All	Current Consumption 2 MSB		
244 (page 03)	All	Current Consumption 2 MSB		

3.7.8 Programmable Power Dissipation and Thermal Emulation

The consumed power changes accordingly when the value of the power control registers changed (only when in high power mode). In Low power mode the module automatically turns off all power spots.
The values written in these registers are permanently stored. The power spots can also be used for module thermal emulation. All registers are in upper page 03.

Register	Bit	Control Type	Description	Default Value	Memory Type
247	7:0	Programmable	Spot 1 at the Top Controlled From 0 to 255	7.5 W	RW (NVR)
248	7:0	Programmable	Spot 2 at the Top Controlled From 0 to 255	7.5 W	
249	7:0	Programmable	Spot 3 at the Top Controlled From 0 to 255	7.5 W	
250	7:0	Programmable	Spot 4 at the Top Controlled From 0 to 255	7.5 W	
251	7:0	Programmable	Spot 5 at the Bottom Controlled From 0 to 255	7.5 W	
252	7:0	Programmable	Spot 6 at the Bottom Controlled From 0 to 255	7.5 W	

The power spots distribution is shown in the image below:

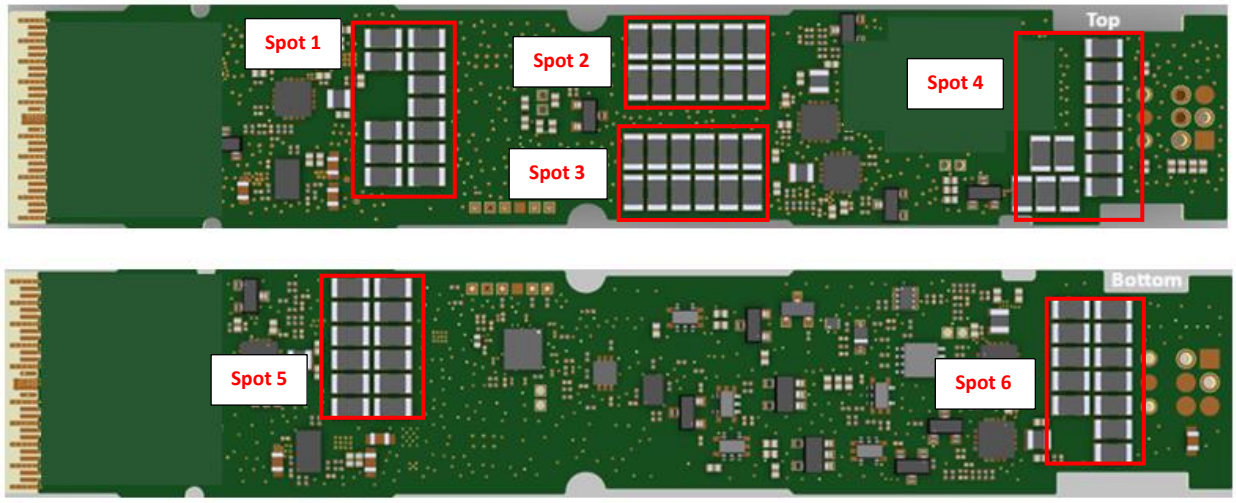


Figure 7: Power Spots Distribution

3.7.9 Low Speed Signals Pin Status

The register below is accessed from page 03h.

Register	Page	Bit	Name	Description	Memory Type
254	Page 03h	1	LPWn/PRSn	Read 1b: High Read 0b: Low	RO
		4	LPWn pin state transition	Read 0b: No edge detected Read 1b: Either rising edge or falling edge crossing the 1.25V threshold is detected Write 0b: No effect Write 1b: Clear the register	RW

3.7.10 IntL Control

During power-up of the module, INT is defaulted to negated. Afterward, host can set the status of this indicator to any status through an I2C registers **in upper page 03**. Setting it should not affect any operation in the module.

Address	Bit	Name	Description	Type
255	1~0	IntL_CNT	Digital Control of INTL: 00: Normal Operation 10: Force the INTL to logic 0 11: Force the INTL to logic 1	RW

For “Normal Operation”, the INTL is asserted when the alarm or warning is high (VCC or Temperature) and the LED will start blinking. If the INTL_CNT is set from this register, the LED won’t blink.

3.7.11 True Insertion Counter

The true insertion counter contains the number of times the module was plugged in a host. The true insertion counter is incremented every time the module goes in initializing sequence, as it is nonvolatile it is always saved. The true insertion counter can be read from registers 245 and 246 page03.

Address	Page	Name	Description	Type
245	Page 03h	True Insertion Counter MSB		RO
246		True Insertion Counter LSB	LSB unit = 1 insertion	

3.7.12 Maximum Power Indicator

The maximum power in the module is indicated by reading register 201 of Page 00. The value of this register is the maximum power consumption in multiples of 0.25 W rounded up to the next whole multiple of 0.25 W.

Address	Page	Bit	Name	Description	Default	Type
201	Page 00h	All	Max Power Indicator	Module Maximum Power Consumption	In decimal: 180 Corresponding to 45W	RO

3.7.13 Alarm and warning thresholds

Each A/D quantity has a corresponding high alarm, low alarm, high warning and low warning threshold. These factory-preset values allow the user to determine when a particular value is exceeding the predefined limit. While Voltage LSB unit is 100 µV and Temperature LSB unit is 1/256 ˚C.

Address	Page	Bit	Name	Default Value (DEC)	Default Value (HEX)	Type
128	Page 02h	ALL	high temp alarm threshold (MSB)	80˚C	0x50	RO
129		ALL	high temp alarm threshold (LSB)		0x00	
130		ALL	low temp alarm threshold (MSB)	0° C	0x00	
131		ALL	low temp alarm threshold (LSB)		0x00	
132		ALL	high temp warning threshold (MSB)	75˚C	0x4B	
133		ALL	high temp warning threshold (LSB)		0x00	
134		ALL	low temp warning threshold (MSB)	5˚C	0x05	
135		ALL	low temp warning threshold (LSB)		0x00	
136		ALL	high volt alarm threshold (MSB)	3.63 V	0x8D	
137		ALL	high volt alarm threshold (LSB)		0xCC	
138		ALL	low volt alarm threshold (MSB)	2.97 V	0x74	
139		ALL	low volt alarm threshold (LSB)		0x04	
140		ALL	high volt warning threshold (MSB)	3.58 V	0x8B	
141		ALL	high volt warning threshold (LSB)		0xD8	
142		ALL	low volt warning threshold (MSB)	3.02 V	0x75	
143		ALL	low volt warning threshold (LSB)		0xF8	

4. CDB Firmware Upgrade

The generic CDB based firmware update facilities allow hosts to update the module firmware completely in a vendor supported depth and granularity.
The module advertises in page 01h for single CDB instance with autopaging supported with maximum EPL pages of 16 (A0-AFh). The firmware supports only single image update.

Complete commands supported:

- CDB Feature and Capabilities Commands

ID	Command Title
0040h	Module Features advertisement
0041h	Firmware Management Features advertisement
0042h	Performance Monitoring Features advertisement
0043h	BERT and Diagnostic Features advertisement

- CDB Firmware Management Commands

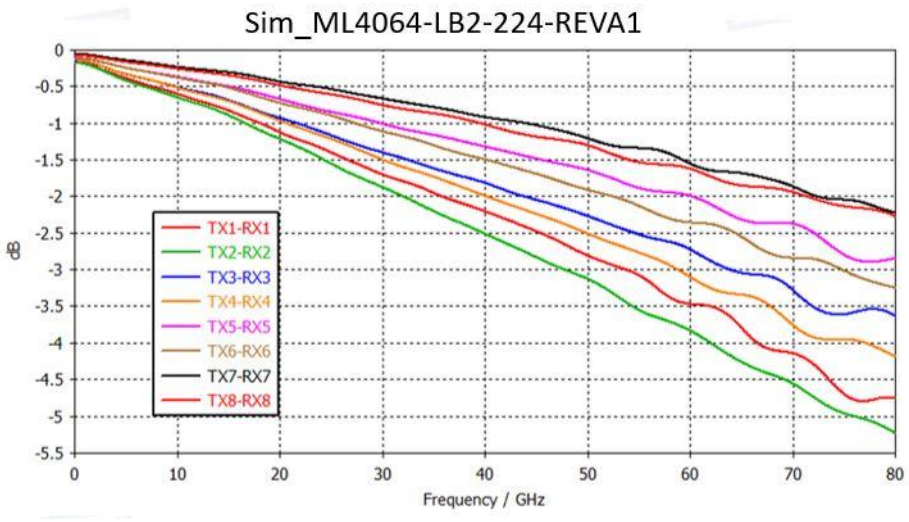
ID	Command Title
0100h	Get Firmware Info command
0101h	Start Firmware Download command
0104h	Write Firmware Block EPL command
0107h	Complete Firmware Download command
0109h	Run Firmware Image command
010Ah	Commit Firmware Image command

5. High Speed Signals

High speed signals are electrically looped back from TX side to RX side of the module, all differential TX pairs are connected to the corresponding RX pairs (straight Mapping).
The signals are DC coupled, there is no AC caps on the module.
The Passive traces connecting TX to RX pairs are designed to support a data rate up to 224Gbps.

5.1 ML4064-LB2-224 Insertion loss graph

The graph below shows the insertion loss simulated data of the ML4064-LB2-224, for all eight channels.



6. OSFP Pin Allocation

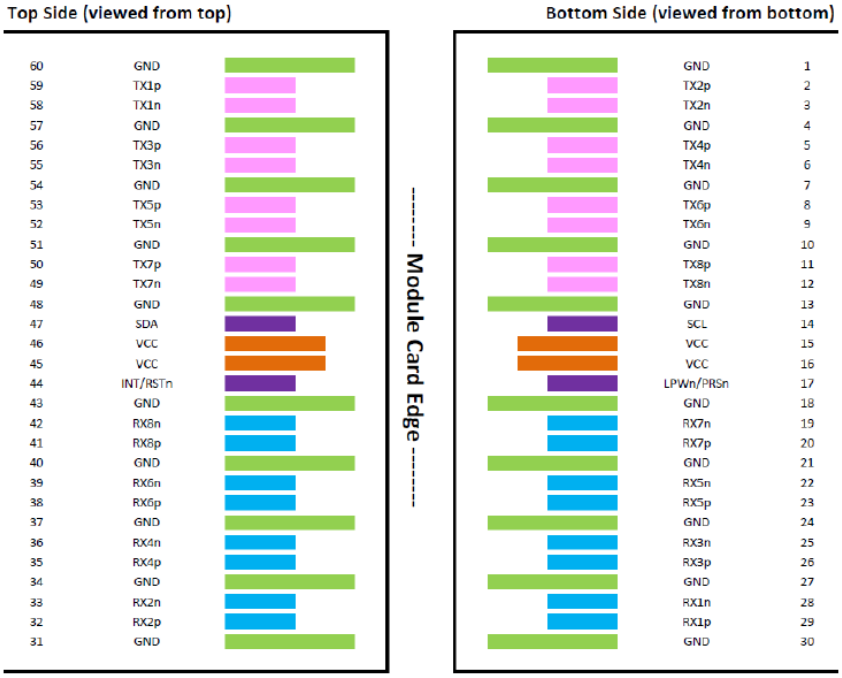


Figure 8: OSFP Module Pad Layout

7. Mechanical Dimensions

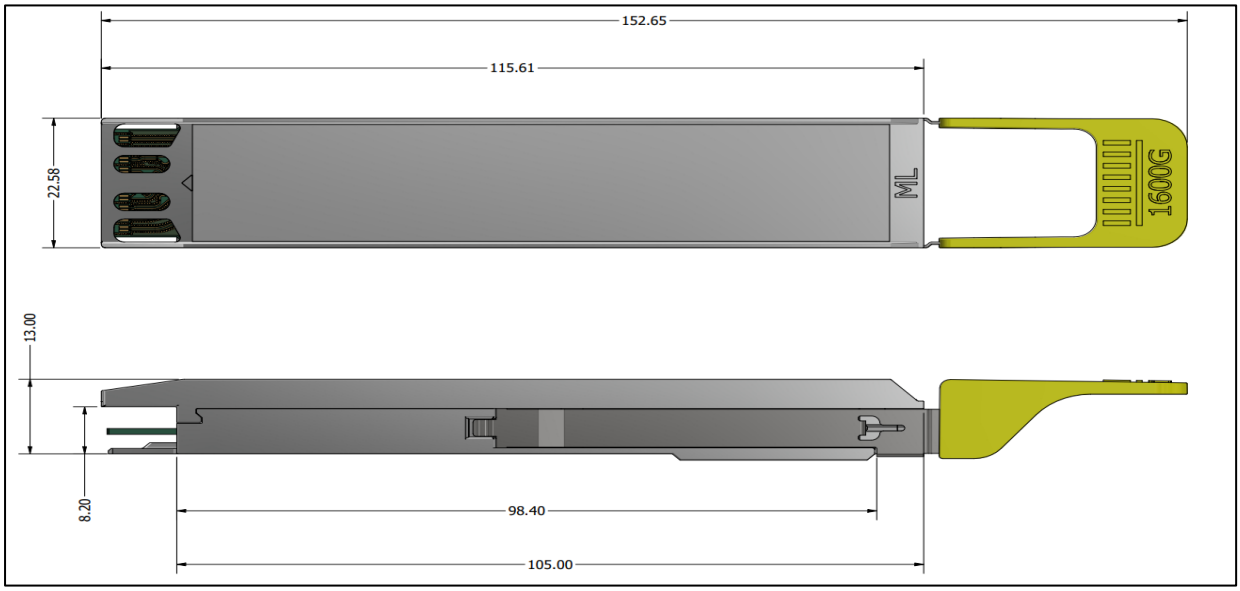


Figure 9: ML4064-LB2I-224

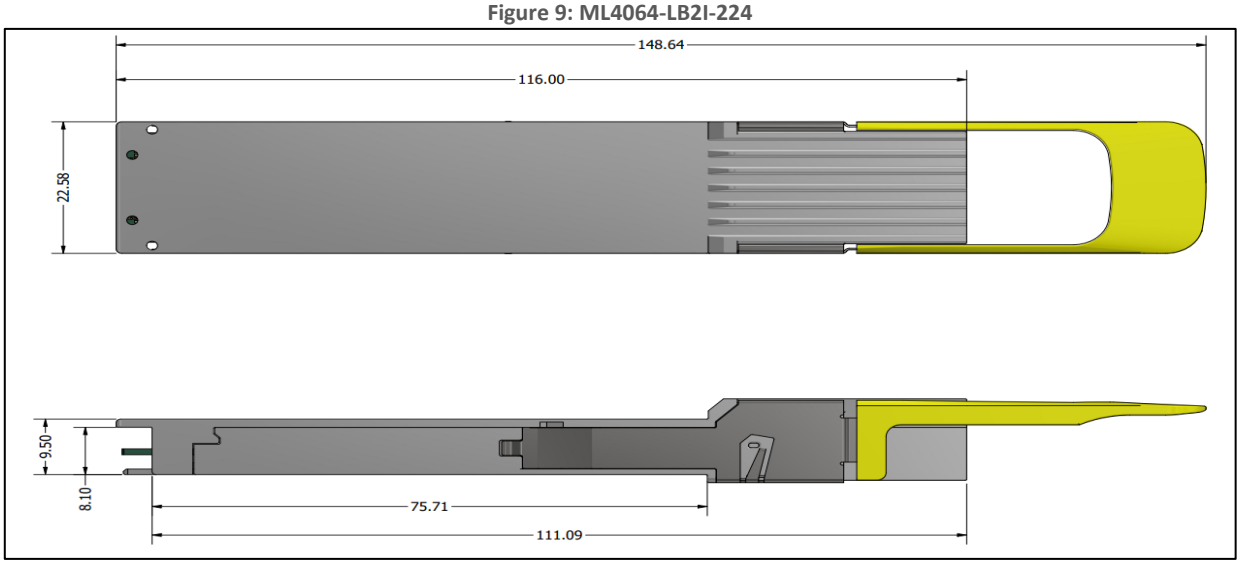


Figure 10: ML4064-LB2R-224

8. Firmware Revision

Rev A1:

FW Release	Upgrades
V1.0	▪ Initial FW release
V1.1	▪ Changing LED behavior

Rev A2:

FW Release	Upgrades
V1.0	▪ Initial FW release

Revision History

Revision number	Date	Description
0.1	3/10/2025	▪ Preliminary
0.2	3/28/2025	▪ Added 2 pictures in the cover page ▪ Adjusted the Memory map table on section 3.4.3 ▪ Adjusted picture ratio on section 3.6.5 ▪ Updated section 3.6.6 ▪ Adjusted pictures on section 3.6.8
0.3	4/2/2025	▪ Updated section 3.6.5 ▪ Updated section 3.6.8
0.4	4/15/2025	▪ Updated section 3.4.3 by changing the value of Reg 145 page 01.
0.5	5/2/2025	▪ Updated section 2.1 by changing the PN ▪ Updated section 3.4.3 by adjusting the Vendor Rev and PN ▪ Updated Section 3.6.6 by adding the default value of the cut-off temp.
0.6	9/17/2025	▪ Removed AC caps mentioning ▪ Updated section 5
0.7	5/21/2026	▪ Adding FW revision ▪ Adding section 3.3 (I3C) ▪ Updated section 3.7.8 picture